WHAT IS CLAIMED IS:

1. A shift overflow detection circuit for a shifter having a data bit length of M and a shift control value bit length of N comprising:

a plurality of circuit elements disposed in M rows and N columns, each circuit element(i,d) of the i-th row and the d-th column having two inputs and an output, a circuit element of a last column generating an output of said shift overflow detection circuit, wherein:

if $d=2^n*2^i$ where n is in the range $1 \le n \le ((M/2^{i+1})-1)$, then element(i,d) is an OR gate having a first input connected to said output of element$(i-1,d+2^i)$ and a second input connected to said output of element(i-1,d),

if $d=2^n*2^i+2^j$ where n is in the range $1 \le n \le ((M/2^{i+1})-1)$ and j is in the range $0 \le j \le i-1$, then element(i,d) is a multiplexer having a first input connected to said output of element(i-1,d), a second input connected to said output of element$(i-1,d+2^i)$ and a control input receiving the i-bit of said shift control value,

if $d=(2^n+1)*2^i$, where n is in the range $1 \le n \le ((M/2^{i+1})-1)$ and j is in the range $0 \le j \le i-1$, then element(i,d) is a multiplexer having a first input connected to said output of element(i-1,d), a second input receiving 0 and a control input receiving the i-bit of said shift control value, and

for all other combinations of i and d, there is no element(i,d).

1   2. The shift overflow detector of claim 1, wherein:
2   each multiplexer includes
3   a first pass gate having a input connected to said
4   first input of said multiplexer, an output connected to
5   said output of said multiplexer and receiving said control
6   input in a first polarity whereby said first pass gate is
7   conducting when said control input is 1, and
8   a second pass gate having a input connected to said
9   second input of said multiplexer, an output connected to
10   said output of said multiplexer and receiving said control
11   input in a second polarity opposite to said first polarity
12   whereby said first pass gate is conducting when said
13   control input is 0.

1   3. A shift overflow detection circuit having a 16 bit data
2   length [D15:D0] and a shift control value of 4 bits [S3:S0],
3   comprising:
4   a first multiplexer having a first input receiving data bit
5   D1, a second input receiving 0, a control input receiving shift
6   value bit S0 and an output;
7   a first OR gate having a first input receiving data bit D2,
8   a second input receiving data bit D3 and an output;
9   a second multiplexer having a first input receiving data
10   bit D3, a second input receiving 0, a control input receiving
11   shift value bit S0 and an output;
12   a second OR gate having a first input receiving data bit
13   D4, a second input receiving data bit D5 and an output;
14   a third multiplexer having a first input receiving data bit
15   D5, a second input receiving 0, a control input receiving shift
16   value bit S0 and an output;

17   a third OR gate having a first input receiving data bit D6,
18   a second input receiving data bit D7 and an output;
19   a fourth multiplexer having a first input receiving data
20   bit D7, a second input receiving 0, a control input receiving
21   shift value bit S0 and an output;
22   a fourth OR gate having a first input receiving data bit
23   D8, a second input receiving data bit D9 and an output;
24   a fifth multiplexer having a first input receiving data bit
25   D9, a second input receiving 0, a control input receiving shift
26   value bit S0 and an output;
27   a fifth OR gate having a first input receiving data bit
28   D10, a second input receiving data bit D11 and an output;
29   a sixth multiplexer having a first input receiving data bit
30   D11, a second input receiving 0, a control input receiving shift
31   value bit S0 and an output;
32   a sixth OR gate having a first input receiving data bit
33   D12, a second input receiving data bit D13 and an output;
34   a seventh multiplexer having a first input receiving data
35   bit D13, a second input receiving 0, a control input receiving
36   shift value bit S0 and an output;
37   a seventh OR gate having a first input receiving data bit
38   D14, a second input receiving data bit D15 and an output;
39   an eighth multiplexer having a first input receiving data
40   bit D15, a second input receiving 0, a control input receiving
41   shift value bit S0 and an output;
42   a ninth multiplexer having a first input connected to said
43   output of said first multiplexer, a second input connected to
44   said output of said second multiplexer, a control input
45   receiving shift control value bit S1 and an output;

46   a tenth multiplexer having a first input connected to said
47   output of said first OR gate, a second input receiving 0, a
48   control input receiving shift control value bit S1 and an
49   output;

50   an eighth OR gate having a first input connected to said
51   output of said second OR gate, a second output connected to said
52   output of said third OR gate and an output;

53   an eleventh multiplexer having a first input connected to
54   said output of said third multiplexer, a second input connected
55   to said output of said fourth multiplexer, a control input
56   receiving shift control value bit S1 and an output;

57   a twelfth multiplexer having a first input connected to
58   said output of said third OR gate, a second input receiving 0, a
59   control input receiving shift control value bit S1 and an
60   output;

61   a ninth OR gate having a first input connected to said
62   output of said fourth OR gate, a second output connected to said
63   output of said fifth OR gate and an output;

64   a thirteenth multiplexer having a first input connected to
65   said output of said fifth multiplexer, a second input connected
66   to said output of said sixth multiplexer, a control input
67   receiving shift control value bit S1 and an output;

68   a fourteenth multiplexer having a first input connected to
69   said output of said fifth OR gate, a second input receiving 0, a
70   control input receiving shift control value bit S1 and an
71   output;

72   a tenth OR gate having a first input connected to said
73   output of said sixth OR gate, a second output connected to said
74   output of said seventh OR gate and an output;

75   a fifteenth multiplexer having a first input connected to
76 said output of said seventh multiplexer, a second input
77 connected to said output of said eighth multiplexer, a control
78 input receiving shift control value bit S1 and an output;

79   a sixteenth multiplexer having a first input connected to
80 said output of said seventh OR gate, a second input receiving 0,
81 a control input receiving shift control value bit S1 and an
82 output;

83   a seventeenth multiplexer having a first input connected to
84 said output of said ninth multiplexer, a second input connected
85 to said output of said eleventh multiplexer, a control input
86 receiving shift control value bit S2 and an output;

87   an eighteenth multiplexer having a first input connected to
88 said output of said tenth multiplexer, a second input connected
89 to said output of said twelfth multiplexer, a control input
90 receiving shift control value bit S2 and an output;

91   a nineteenth multiplexer having a first input connected to
92 said output of said eighth OR gate, a second input receiving 0,
93 a control input receiving shift control value bit S2 and an
94 output;

95   an eleventh OR gate having a first input connected to said
96 output of said ninth OR gate, a second output connected to said
97 output of said tenth OR gate and an output;

98   a twentieth multiplexer having a first input connected to
99 said output of said thirteenth multiplexer, a second input
100 connected to said output of said fifteenth multiplexer, a
101 control input receiving shift control value bit S2 and an
102 output;

103   a twenty first multiplexer having a first input connected
104 to said output of said fourteenth multiplexer, a second input

105 connected to said output of said sixteenth multiplexer, a
106 control input receiving shift control value bit S2 and an
107 output;

108   a twenty second multiplexer having a first input connected
109 to said output of said tenth OR gate, a second input receiving
110 0, a control input receiving shift control value bit S2 and an
111 output;

112   a twenty third multiplexer having a first input connected
113 to said output of said seventeenth multiplexer, a second input
114 connected to said output of said twentieth multiplexer, a
115 control input receiving shift control value bit S3 and an
116 output;

117   a twenty fourth multiplexer having a first input connected
118 to said output of said eighteenth multiplexer, a second input
119 connected to said output of said twenty first multiplexer, a
120 control input receiving shift control value bit S3 and an
121 output;

122   a twenty fifth multiplexer having a first input connected
123 to said output of said nineteenth multiplexer, a second input
124 connected to said output of said twenty second multiplexer, a
125 control input receiving shift control value bit S3 and an
126 output;

127   a twenty sixth multiplexer having a first input connected
128 to said output of said eleventh OR gate, a second input
129 receiving 0, a control input receiving shift control value bit
130 S3 and an output;

131   a twelfth OR gate having a first input connected to said
132 output of said twenty third multiplexer, a second input
133 connected to said output of said twenty fourth multiplexer and
134 an output;

135   a thirteenth OR gate having a first input connected to said
136 output of said twenty fifth multiplexer, a second input
137 connected to said output of said twenty sixth multiplexer and an
138 output; and

139   a fourteenth OR gate having a first input connected to said
140 output of said twelfth OR gate, a second input connected to said
141 output of said thirteenth OR gate and an output forming an
142 output of said shift overflow detection circuit.

1   4.   The shift overflow detector of claim 2, wherein:
2 each of said first to twenty sixth multiplexer includes
3   a first pass gate having a input connected to said
4 first input of said multiplexer, an output connected to
5 said output of said multiplexer and receiving said control
6 input in a first polarity whereby said first pass gate is
7 conducting when said control input is 1, and
8   a second pass gate having a input connected to said
9 second input of said multiplexer, an output connected to
10 said output of said multiplexer and receiving said control
11 input in a second polarity opposite to said first polarity
12 whereby said first pass gate is conducting when said
13 control input is 0.

1   5.   A shift overflow detection circuit having a 32 bit data
2 length [D31:D0] and a shift control value of 5 bits [S4:S0],
3 comprising:
4   a first multiplexer having a first input receiving data bit
5 D1, a second input receiving data bit D3, a control input
6 receiving shift control value bit S1 and an output;

7   a first NAND gate having a first input connected to said
8 output of said first multiplexer, a second input receiving shift
9 control value bit S0 and an output;

10   a first OR gate having a first input receiving data bit D2,
11 a second input receiving data bit D3 and an output;

12   a second NAND gate having a first input connected to said
13 output of said first OR gate, a second input receiving shift
14 control value bit S0 and an output;

15   a first NOR gate having a first input receiving data bit
16 D4, a second input receiving data bit D5 and an output;

17   a second multiplexer having a first input receiving data
18 bit D5, a second input receiving data bit D7, a control input
19 receiving shift control value bit S1 and an output;

20   a third NAND gate having a first input connected to said
21 output of said second multiplexer, a second input receiving
22 shift control value bit S0 and an output;

23   a second NOR gate having a first input receiving data bit
24 D6, a second input receiving data bit D7 and an output;

25   a second OR gate having a first input receiving data bit
26 D6, a second input receiving data bit D7 and an output;

27   a fourth NAND gate having a first input connected to said
28 output of said second OR gate, a second input receiving shift
29 control value bit S0 and an output;

30   a third NOR gate having a first input receiving data bit
31 D8, a second input receiving data bit D9 and an output;

32   a third multiplexer having a first input receiving data bit
33 D9, a second input receiving data bit D11, a control input
34 receiving shift control value bit S1 and an output;

35   a fifth NAND gate having a first input connected to said
36 output of said third multiplexer, a second input receiving shift
37 control value bit S0 and an output;

38   a fourth NOR gate having a first input receiving data bit
39 D10, a second input receiving data bit D11 and an output;

40   a third OR gate having a first input receiving data bit
41 D10, a second input receiving data bit D11 and an output;

42   a sixth NAND gate having a first input connected to said
43 output of said third OR gate, a second input receiving shift
44 control value bit S0 and an output;

45   a fifth NOR gate having a first input receiving data bit
46 D12, a second input receiving data bit D13 and an output;

47   a fourth multiplexer having a first input receiving data
48 bit D13, a second input receiving data bit D15, a control input
49 receiving shift control value bit S1 and an output;

50   a seventh NAND gate having a first input connected to said
51 output of said fourth multiplexer, a second input receiving
52 shift control value bit S0 and an output;

53   a sixth NOR gate having a first input receiving data bit
54 D14, a second input receiving data bit D15 and an output;

55   a fourth OR gate having a first input receiving data bit
56 D14, a second input receiving data bit D15 and an output;

57   an eighth NAND gate having a first input connected to said
58 output of said fourth OR gate, a second input receiving shift
59 control value bit S0 and an output;

60   a seventh NOR gate having a first input receiving data bit
61 D16, a second input receiving data bit D17 and an output;

62   a fifth multiplexer having a first input receiving data bit
63 D17, a second input receiving data bit D19, a control input
64 receiving shift control value bit S1 and an output;

65   a ninth NAND gate having a first input connected to said
66 output of said fifth multiplexer, a second input receiving shift
67 control value bit S0 and an output;

68   an eighth NOR gate having a first input receiving data bit
69 D18, a second input receiving data bit D19 and an output;

70   a fifth OR gate having a first input receiving data bit
71 D18, a second input receiving data bit D19 and an output;

72   a tenth NAND gate having a first input connected to said
73 output of said fifth OR gate, a second input receiving shift
74 control value bit S0 and an output;

75   a ninth NOR gate having a first input receiving data bit
76 D20, a second input receiving data bit D21 and an output;

77   a sixth multiplexer having a first input receiving data bit
78 D21, a second input receiving data bit D23, a control input
79 receiving shift control value bit S1 and an output;

80   an eleventh NAND gate having a first input connected to
81 said output of said sixth multiplexer, a second input receiving
82 shift control value bit S0 and an output;

83   a tenth NOR gate having a first input receiving data bit
84 D22, a second input receiving data bit D23 and an output;

85   a sixth OR gate having a first input receiving data bit
86 D22, a second input receiving data bit D23 and an output;

87   a twelfth NAND gate having a first input connected to said
88 output of said sixth OR gate, a second input receiving shift
89 control value bit S0 and an output;

90   an eleventh NOR gate having a first input receiving data
91 bit D24, a second input receiving data bit D25 and an output;

92   a seventh multiplexer having a first input receiving data
93 bit D25, a second input receiving data bit D27, a control input
94 receiving shift control value bit S1 and an output;

95   a thirteenth NAND gate having a first input connected to
96 said output of said seventh multiplexer, a second input
97 receiving shift control value bit S0 and an output;

98   a twelfth NOR gate having a first input receiving data bit
99 D26, a second input receiving data bit D27 and an output;

100   a seventh OR gate having a first input receiving data bit
101 D26, a second input receiving data bit D27 and an output;

102   a fourteenth NAND gate having a first input connected to
103 said output of said seventh OR gate, a second input receiving
104 shift control value bit S0 and an output;

105   a thirteenth NOR gate having a first input receiving data
106 bit D28, a second input receiving data bit D29 and an output;

107   an eighth multiplexer having a first input receiving data
108 bit D29, a second input receiving data bit D31, a control input
109 receiving shift control value bit S1 and an output;

110   a fifteenth NAND gate having a first input connected to
111 said output of said eighth multiplexer, a second input receiving
112 shift control value bit S0 and an output;

113   a fourteenth NOR gate having a first input receiving data
114 bit D30, a second input receiving data bit D31 and an output;

115   an eighth OR gate having a first input receiving data bit
116 D30, a second input receiving data bit D31 and an output;

117   a sixteenth NAND gate having a first input connected to
118 said output of said eighth OR gate, a second input receiving
119 shift control value bit S0 and an output;

120   a seventeenth NAND gate having a first input connected to
121 said output of said first NAND gate, a second input connected to
122 said output of said second NAND gate, a third input connected to
123 said output of said first NOR gate, a fourth input connected to
124 said output of said second NOR gate and an output;

125   an eighteenth NAND gate having a first input connected to
126 said output of said third NAND gate, a second input connected to
127 said output of said fourth NAND gate and an output;

128   a nineteenth NAND gate having a first input connected to
129 said output of said third NOR gate, a second input connected to
130 said output of said fourth NOR gate, a third input connected to
131 said output of said fifth NOR gate, a fourth input connected to
132 said output of said sixth NOR gate and an output;

133   a twentieth NAND gate having a first input connected to
134 said output of said fifth NAND gate, a second input connected to
135 said output of said sixth NAND gate, a third input connected to
136 said output of said fifth NOR gate, a fourth input connected to
137 said output of said sixth NOR gate and an output;

138   a twenty first NAND gate having a first input connected to
139 said output of said seventh NAND gate, a second input connected
140 to said output of said eighth NAND gate and an output;

141   a twenty second NAND gate having a first input connected to
142 said output of said seventh NOR gate, a second input connected
143 to said output of said eighth NOR gate, a third input connected
144 to said output of said ninth NOR gate, a fourth input connected
145 to said output of said tenth NOR gate and an output;

146   a twenty third NAND gate having a first input connected to
147 said output of said ninth NAND gate, a second input connected to
148 said output of said tenth NAND gate, a third input connected to
149 said output of said ninth NOR gate, a fourth input connected to
150 said output of said tenth NOR gate and an output;

151   a twenty fourth NAND gate having a first input connected to
152 said output of said eleventh NAND gate, a second input connected
153 to said output of said twelfth NAND gate and an output;

154   a twenty fifth NAND gate having a first input connected to
155 said output of said eleventh NOR gate, a second input connected
156 to said output of said twelfth NOR gate, a third input connected
157 to said output of said thirteenth NOR gate, a fourth input
158 connected to said output of said fourteenth NOR gate and an
159 output;

160   a twenty sixth NAND gate having a first input connected to
161 said output of said thirteenth NAND gate, a second input
162 connected to said output of said fourteenth NAND gate, a third
163 input connected to said output of said thirteenth NOR gate, a
164 fourth input connected to said output of said fourteenth NOR
165 gate and an output;

166   a twenty seventh NAND gate having a first input connected
167 to said output of said fifteenth NAND gate, a second input
168 connected to said output of said sixteenth NAND gate and an
169 output;

170   a seventeenth multiplexer having a first input connected to
171 said output of said nineteenth NAND gate, a second input
172 connected to said twenty fifth NAND gate, a control input
173 receiving shift control value bit S4 and an output;

174   a twenty eighth NAND gate having a first input connected to
175 said output of said seventeenth multiplexer, a second input
176 receiving shift control value bit S3 and an output;

177   a ninth OR gate having a first input connected to said
178 output of said twenty second NAND gate, a second input connected
179 to said output of said twenty fifth NAND gate and an output;

180   a twenty ninth NAND gate having a first input connected to
181 said output of said ninth OR gate, a second input receiving
182 shift control value bit S4 and an output;

183   an inverting multiplexer having a first input connected to
184   said output of said seventeenth NAND gate, a second input
185   connected to said output of said eighteenth NAND gate, a third
186   input connected to said output of said twentieth NAND gate, a
187   fourth input connected to said output of said twenty first NAND
188   gate, a fifth input connected to said output of said twenty
189   third NAND gate, a sixth input connected to said output of said
190   twenty fourth NAND gate, a seventh input connected to said
191   output of said twenty sixth NAND gate, an eighth input connected
192   to said output of said twenty seventh NAND gate, three control
193   input receiving respective shift control value bits S4, S3 and
194   S2 and an output, whereby said inverting multiplexer outputs a
195   inverted first input if said shift control bits S4, S3 and S2
196   are "111", a inverted second input if said shift control bits
197   S4, S3 and S2 are "110", a inverted third input if said shift
198   control bits S4, S3 and S2 are "101", a inverted fourth input if
199   said shift control bits S4, S3 and S2 are "100", a inverted
200   fifth input if said shift control bits S4, S3 and S2 are "011",
201   a inverted sixth input if said shift control bits S4, S3 and S2
202   are "010", a inverted seventh input if said shift control bits
203   S4, S3 and S2 are "001" and a inverted eighth input if said
204   shift control bits S4, S3 and S2 are "000"; and
205   a thirtieth NAND gate having a first input connected to
206   said output of said inverting multiplexer, a second input
207   connected to said output of said twenty eighth NAND gate, a
208   third input connected to said output of said twenty ninth NAND
209   gate and an output forming an output of said shift overflow
210   detection circuit.

1   6. The shift overflow detector of claim 5, wherein:
2   each of said first to seventeenth multiplexer includes
3   a first pass gate having a input connected to said
4   first input of said multiplexer, an output connected to
5   said output of said multiplexer and receiving said control
6   input in a first polarity whereby said first pass gate is
7   conducting when said control input is 1, and
8   a second pass gate having a input connected to said
9   second input of said multiplexer, an output connected to
10   said output of said multiplexer and receiving said control
11   input in a second polarity opposite to said first polarity
12   whereby said first pass gate is conducting when said
13   control input is 0.

1   7. The shift overflow detector of claim 5, wherein:
2   said inverting multiplexer includes
3   a first inverter having a input receiving shift
4   control value bit S2 and an output,
5   a second inverter having a input receiving shift
6   control value bit S3 and an output,
7   a third inverter having a input receiving shift
8   control value bit S4 and an output,
9   a first NAND gate having a first input receiving shift
10   control value S2, a second input receiving shift control
11   value S3, a third input receiving shift control value S4
12   and an output,
13   a second NAND gate having a first input connected to
14   said output of said first inverter, a second input
15   receiving shift control value S3, a third input receiving
16   shift control value S4 and an output,

17   a third NAND gate having a first input receiving shift
18 control value S2, a second input connected to said output
19 of said second inverter, a third input receiving shift
20 control value S4 and an output,
21   a fourth NAND gate having a first input connected to
22 said output of said first inverter, a second input
23 connected to said output of said second inverter, a third
24 input receiving shift control value S4 and an output,
25   . a fifth NAND gate having a first input receiving shift
26 control value S2, a second input receiving shift control
27 value S3, a third input connected to said output of said
28 third inverter and an output,
29   a sixth NAND gate having a first input connected to
30 said output of said first inverter, a second input
31 receiving shift control value S3, a third input connected
32 to said output of said third inverter and an output,
33   a seventh NAND gate having a first input receiving
34 shift control value S2, a second input connected to said
35 output of said second inverter, a third input connected to
36 said output of said third inverter and an output,
37   . a eighth NAND gate having a first input connected to
38 said output of said first inverter, a second input
39 connected to said output of said second inverter, a third
40 input connected to said output of said third inverter and
41 an output,
42   a fourth inverter having an input connected to said
43 output of said first NAND gate and an output,
44   a fifth inverter having an input connected to said
45 output of said second NAND gate and an output,

46   a sixth inverter having an input connected to said
47 output of said third NAND gate and an output,
48   a seventh inverter having an input connected to said
49 output of said fourth NAND gate and an output,
50   a eighth inverter having an input connected to said
51 output of said fifth NAND gate and an output,
52   a ninth inverter having an input connected to said
53 output of said sixth NAND gate and an output,
54   a tenth inverter having an input connected to said
55 output of said seventh NAND gate and an output,
56   a eleventh inverter having an input connected to said
57 output of said eighth NAND gate and an output,
58   a first pass gate having an input connected to said
59 first input of said inverting multiplexer, a first control
60 input connected to said output of said first NAND gate, a
61 second control input connected to said output of said
62 fourth inverter and an output,
63   a second pass gate having an input connected to said
64 second input of said inverting multiplexer, a first control
65 input connected to said output of said second NAND gate, a
66 second control input connected to said output of said fifth
67 inverter and an output,
68   a third pass gate having an input connected to said
69 third input of said inverting multiplexer, a first control
70 input connected to said output of said third NAND gate, a
71 second control input connected to said output of said sixth
72 inverter and an output,
73   a fourth pass gate having an input connected to said
74 fourth input of said inverting multiplexer, a first control
75 input connected to said output of said fourth NAND gate, a

76   second control input connected to said output of said
77   seventh inverter and an output,

78   a fifth pass gate having an input connected to said
79   fifth input of said inverting multiplexer, a first control
80   input connected to said output of said fifth NAND gate, a
81   second control input connected to said output of said
82   eighth inverter and an output,

83   a sixth pass gate having an input connected to said
84   sixth input of said inverting multiplexer, a first control
85   input connected to said output of said sixth NAND gate, a
86   second control input connected to said output of said ninth
87   inverter and an output,

88   a seventh pass gate having an input connected to said
89   seventh input of said inverting multiplexer, a first
90   control input connected to said output of said seventh NAND
91   gate, a second control input connected to said output of
92   said tenth inverter and an output,

93   an eighth pass gate having an input connected to said
94   eighth input of said inverting multiplexer, a first control
95   input connected to said output of said eighth NAND gate, a
96   second control input connected to said output of said
97   eleventh inverter and an output, and

98   a twelfth inverter having an input connected to said
99   output of said first, second, third, fourth, fifth, sixth,
100 seventh and eighth pass gates and an output forming said
101 output of said inverting multiplexer.